IXYS | IXDN404 / IXDI404 / IXDF404

4 Ampere Dual Low-Side Ultrafast MOSFET Drivers

Features

- Built using the advantages and compatibility of CMOS and IXYS HDMOS™ processes
- Latch-Up Protected up to 0.5A
- High Peak Output Current: 4A Peak
- Wide Operating Range: 4.5V to 35V
- High Capacitive Load Drive Capability: 1800pF in <15ns
- Matched Rise And Fall Times
- Low Propagation Delay Time
- Low Output Impedance
- Low Supply Current
- Two Drivers in Single Chip

Applications

- Driving MOSFETs and IGBTs
- Motor Controls
- Line Drivers
- Pulse Generators
- Local Power ON/OFF Switch
- Switch Mode Power Supplies (SMPS)
- DC to DC Converters
- Pulse Transformer Driver
- Class D Switching Amplifiers
- Limiting di/dt Under Short Circuit

General Description

The IXDN404/IXDI404/IXDF404 is comprised of two 4 Ampere CMOS high speed MOSFET drivers. Each output can source and sink 4A of peak current while producing voltage rise and fall times of less than 15ns to drive the latest IXYS MOSFETs and IGBT's. The input of the driver is compatible with TTL or CMOS and is fully immune to latch up over the entire operating range. A patent-pending circuit virtually eliminates CMOS power supply cross conduction and current shoot-through. Improved speed and drive capabilities are further enhanced by very low, matched rise and fall times.

The IXDN404 is configured as a dual non-inverting gate driver, the IXDI404 is a dual inverting gate driver, and the IXDF404 is a dual inverting + non-inverting gate driver.

The IXDN404/IXDI404/IXDF404 family are available in the standard 8 pin P-DIP (PI), SOIC-8 (SIA) and SOIC-16 (SIA-16) packages. For enhanced thermal performance, the SOP-8 and SOP-16 are also available in a package with an exposed grounded metal back as the SI and SI-16 repectively.

Ordering Information

Part Number	Package Type	Temp. Range	Configuration
IXDN404PI	8-Pin PDIP	-55°C to +125°C	Dual Non Inverting
IXDN404SI	8-Pin SOIC with Grounded Metal Back		
IXDN404SIA	8-Pin SOIC		
IXDN404SI-16	16-Pin SOIC with Grounded Metal Back		
IXDN404SIA-16	16-Pin SOIC		
IXDI404PI	8-Pin PDIP	-55°C to +125°C	Dual Inverting
IXDI404SI	8-Pin SOIC with Grounded Metal Back		
IXDI404SIA	8-Pin SOIC		
IXDI404SI-16	16-Pin SOIC with Grounded Metal Back		
IXDI404SIA-16	16-Pin SOIC		
IXDF404PI	8-Pin PDIP	-55°C to +125°C	Inverting + Non Inverting
IXDF404SI	8-Pin SOIC with Grounded Metal Back		
IXDF404SIA	8-Pin SOIC		
IXDF404SI-16	16-Pin SOIC with Grounded Metal Back		
IXDF404SIA-16	16-Pin SOIC		

NOTE: Mounting or solder tabs on all packages are connected to ground

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Figure 1 - IXDN404 Dual 4A Non-Inverting Gate Driver Functional Block Diagram

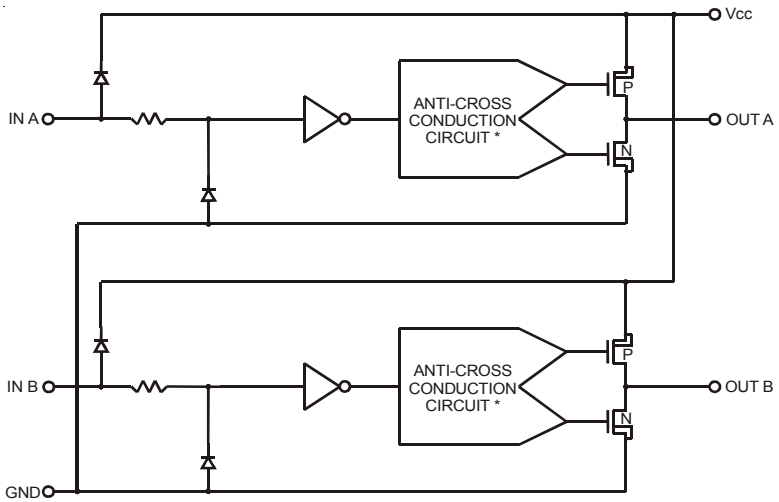


Figure 2 - IXDI404 Dual Inverting 4A Gate Driver Functional Block Diagram

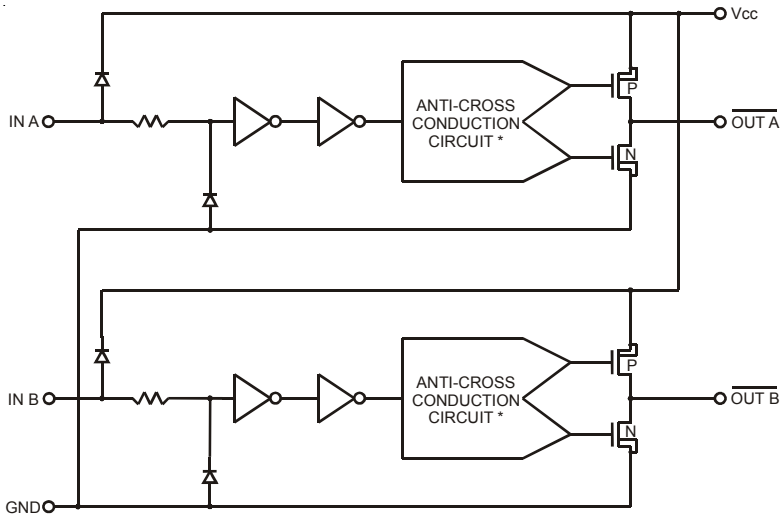
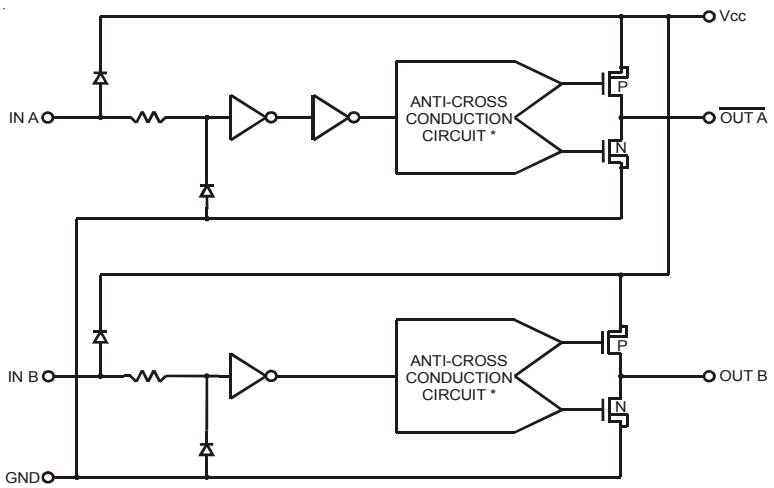


Figure 3 - IXDF404 Inverting + Non-Inverting 4A Gate Driver Functional Block Diagram



* Patent Pending

Absolute Maximum Ratings (Note 1)

Parameter	Value
Supply Voltage	40V
All Other Pins	-0.3V to V_{CC} + 0.3V
Junction Temperature	150°C
Storage Temperature	-65°C to 150°C
Soldering Lead Temperature (10 seconds maximum)	300°C

Thermal Resistance (Junction to Case) (θ_{JC})

8 Pin SOIC (SI)	10 K/W
16 Pin SOIC (SI-16)	10 K/W

Operating Ratings

Parameter	Value
Operating Temperature Range	-55 °C to 125 °C
Thermal Resistance (To Ambient)	
8 Pin PDIP (PI) (θ_{JA})	120 K/W
8 Pin SOIC (SIA)	110 K/W
16 Pin SOIC (SIA-16) (θ_{JA})	110 K/W
θ_{JA} with heat sink **	
Heat sink area of 1 cm^2	
8 Pin SOIC	95 K/W
16 Pin SOIC-CT	95 K/W
Heat sink area of 3 cm^2	
8 Pin SOIC	85 K/W
16 Pin SOIC-CT	85 K/W

** Device soldered to metal back pane. Heat sink area is 1 oz. copper on 1 side of 0.06" thick FR4 PC board.

Electrical Characteristics

Unless otherwise noted, T_A = 25 °C, 4.5V ≤ V_{CC} ≤ 35V .
All voltage measurements with respect to GND. Device configured as described in *Test Conditions.* All specifications are for one channel.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{IH}	High input voltage	4.5V ≤ V_{CC} ≤ 18V	2.5			V
V_{IL}	Low input voltage	4.5V ≤ V_{CC} ≤ 18V			0.8	V
V_{IN}	Input voltage range		-5		V_{CC} + 0.3	V
I_{IN}	Input current	0V ≤ V_{IN} ≤ V_{CC}	-10		10	µA
V_{OH}	High output voltage		V_{CC} - 0.025			V
V_{OL}	Low output voltage				0.025	V
R_{OH}	Output resistance @ Output High	V_{CC} = 18V		2	2.5	Ω
R_{OL}	Output resistance @ Output Low	V_{CC} = 18V		1.5	2	Ω
I_{PEAK}	Peak output current	V_{CC} = 18V		4		A
I_{DC}	Continuous output current				1	A
t_R	Rise time	C_L=1800pF Vcc=18V		16	18	ns
t_F	Fall time	C_L=1800pF Vcc=18V		13	17	ns
t_{ONDLY}	On-time propagation delay	C_L=1800pF Vcc=18V		36	40	ns
t_{OFFDLY}	Off-time propagation delay	C_L=1800pF Vcc=18V		35	39	ns
V_{CC}	Power supply voltage		4.5	18	35	V
I_{CC}	Power supply current	V_{IN} = 3.5V V_{IN} = 0V V_{IN} = + V_{CC}		1 0	3 10 10	mA µA µA

Specifications Subject To Change Without Notice

Note 1: Operating the device beyond parameters with listed "Absolute Maximum Ratings" may cause permanent damage to the device. Typical values indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. The guaranteed specifications apply only for the test conditions listed. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Electrical Characteristics

Unless otherwise noted, temperature over -55°C to 150°C, $4.5V \le V_{CC} \le 35V$.
All voltage measurements with respect to GND. Device configured as described in *Test Conditions*. All specifications are for one channel.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{IH}	High input voltage	$4.5V \le V_{CC} \le 18V$	2.4			V
V_{IL}	Low input voltage	$4.5V \le V_{CC} \le 18V$			0.8	V
V_{IN}	Input voltage range		-5		V_{CC} + 0.3	V
I_{IN}	Input current	$0V \le V_{IN} \le V_{CC}$	-10		10	µA
V_{OH}	High output voltage		V_{CC} - 0.025			V
V_{OL}	Low output voltage				0.025	V
R_{OH}	Output resistance @ Output High	V_{CC} = 18V			3.4	Ω
R_{OL}	Output resistance @ Output Low	V_{CC} = 18V			2	Ω
I_{PEAK}	Peak output current	V_{CC} = 18V		3.2		A
I_{DC}	Continuous output current				1	A
t_R	Rise time	C_L=1000pF Vcc=18V			11	ns
t_F	Fall time	C_L=1000pF Vcc=18V			13	ns
t_{ONDLY}	On-time propagation delay	C_L=1000pF Vcc=18V			60	ns
t_{OFFDLY}	Off-time propagation delay	C_L=1000pF Vcc=18V			59	ns
V_{CC}	Power supply voltage		4.5	18	35	V
I_{CC}	Power supply current	V_{IN} = 3.5V V_{IN} = 0V V_{IN} = + V_{CC}		1 0	3 10 10	mA µA µA

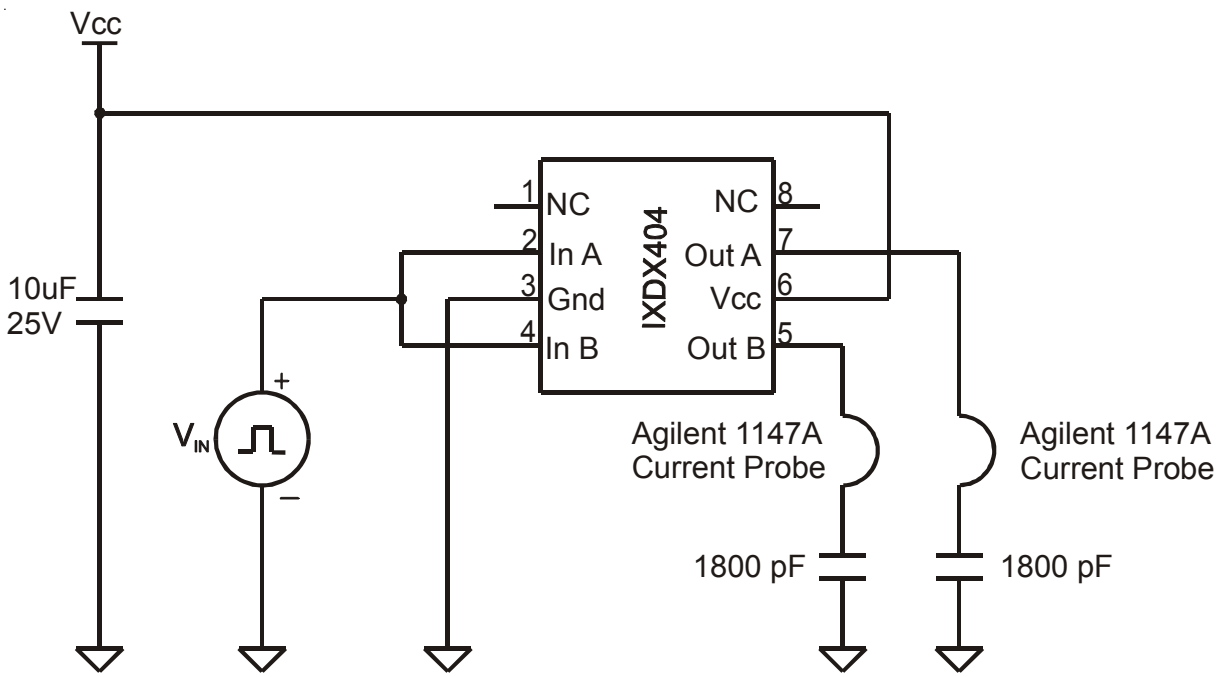
Specifications Subject To Change Without Notice

Pin Description

SYMBOL	FUNCTION	DESCRIPTION
IN A	A Channel Input	A Channel Input signal-TTL or CMOS compatible.
GND	Ground	The system ground pin. Internally connected to all circuitry, this pin provides ground reference for the entire chip. This pin should be connected to a low noise analog ground plane for optimum performance.
IN B	B Channel Input	B Channel Input signal-TTL or CMOS compatible.
OUT B	B Channel Output	B Channel Driver output. For application purposes, this pin is connected via a resistor to a gate of a MOSFET/IGBT.
VCC	Supply Voltage	Positive power-supply voltage input. This pin provides power to the entire chip. The range for this voltage is from 4.5V to 35V.
OUT A	A Channel Output	A Channel Driver output. For application purposes, this pin is connected via a resistor to a gate of a MOSFET/IGBT.

CAUTION: These devices are sensitive to electrostatic discharge; follow proper ESD procedures when handling and assembling this component.

Figure 4 - Characteristics Test Diagram



Typical Performance Characteristics

Fig. 5 Rise Times vs. Supply Voltage

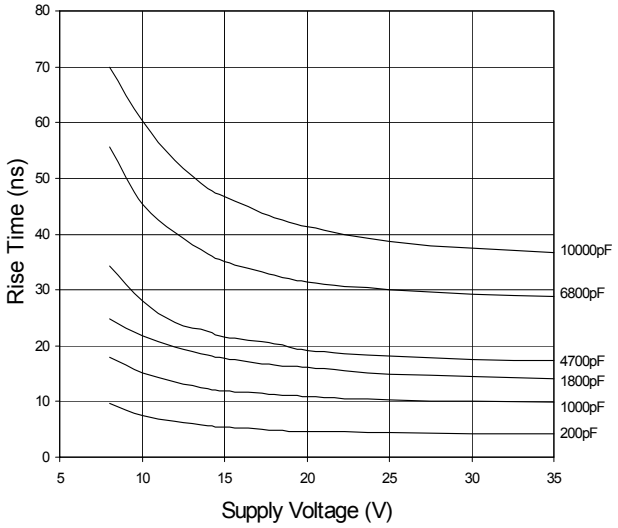


Fig. 6 Fall Times vs. Supply Voltage

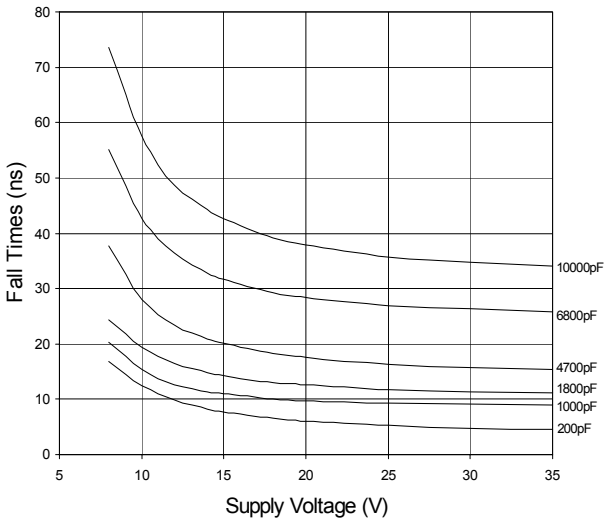


Fig. 7 Output Rise Times vs. Load Capacitance

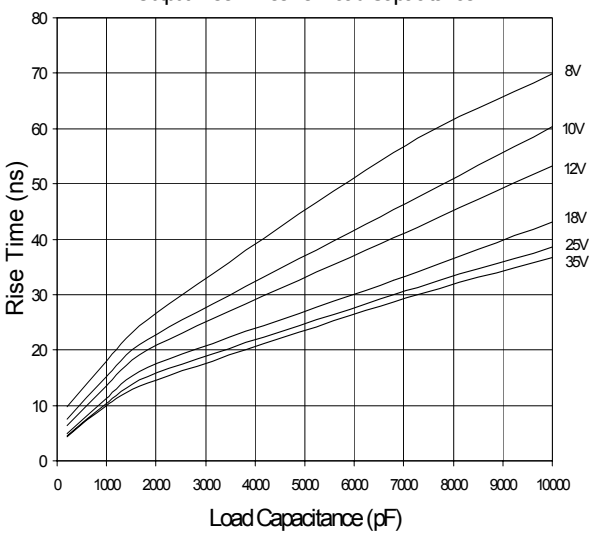


Fig. 8 Output Fall Times vs. Load Capacitance

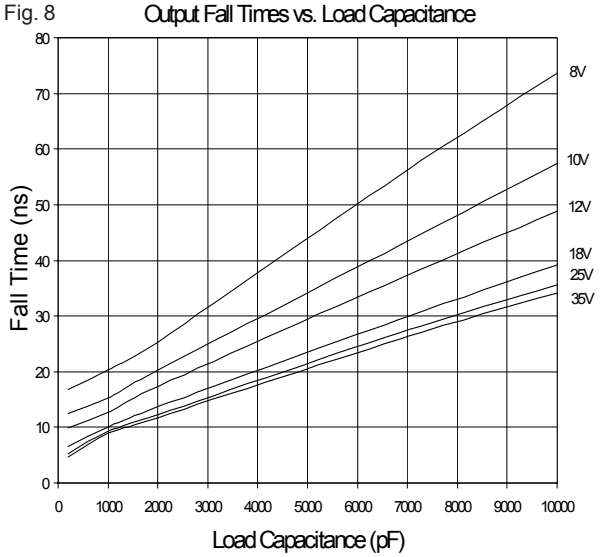


Fig. 9 Rise And Fall Times vs. Temperature
C_L = 1000pF, V_{cc} = 18V

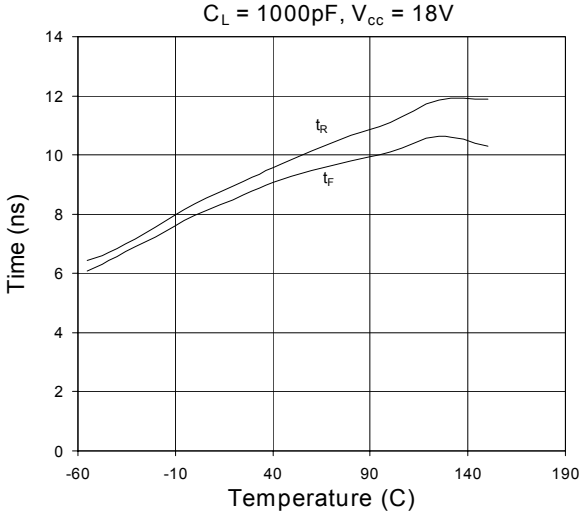


Fig. 10 Max / Min Input vs. Temperature
C_L = 1000pF, V_{cc} = 18V

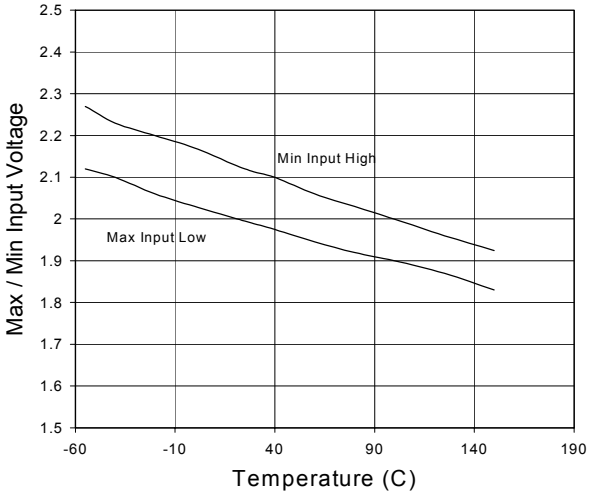


Fig. 11 Supply Current vs. Load Capacitance
Vcc = 8V

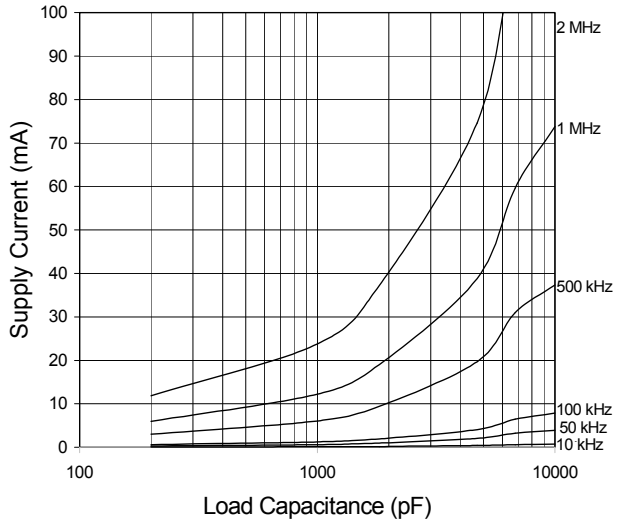


Fig. 12 Supply Current vs. Frequency
Vcc = 8V

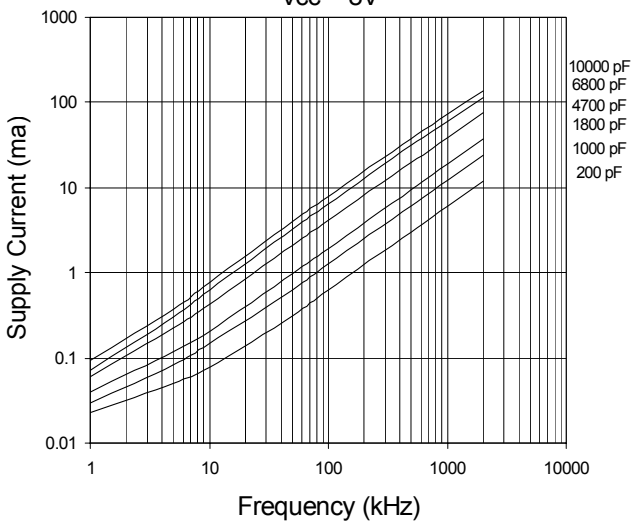


Fig. 13 Supply Current vs. Load Capacitance
Vcc = 12V

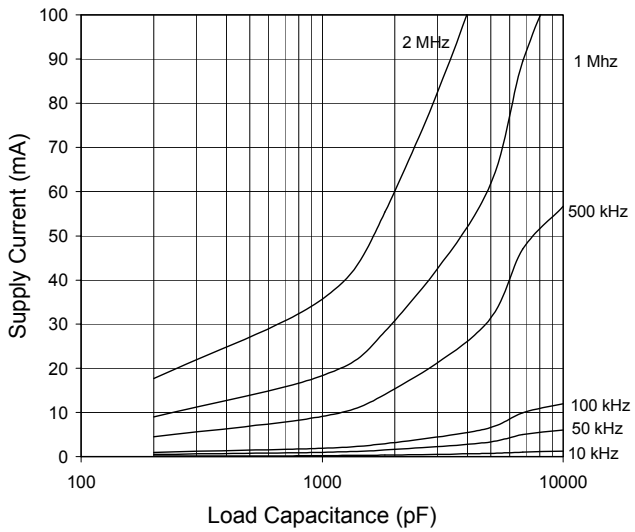


Fig. 14 Supply Current vs. Frequency
Vcc = 12V

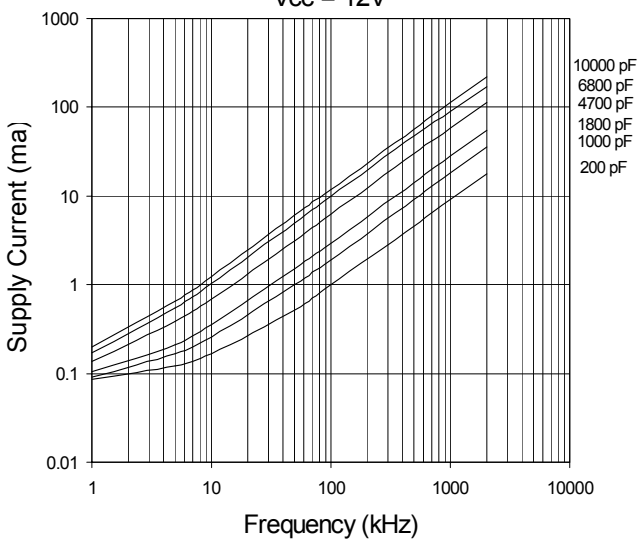


Fig. 15 Supply Current vs. Load Capacitance
Vcc = 18V

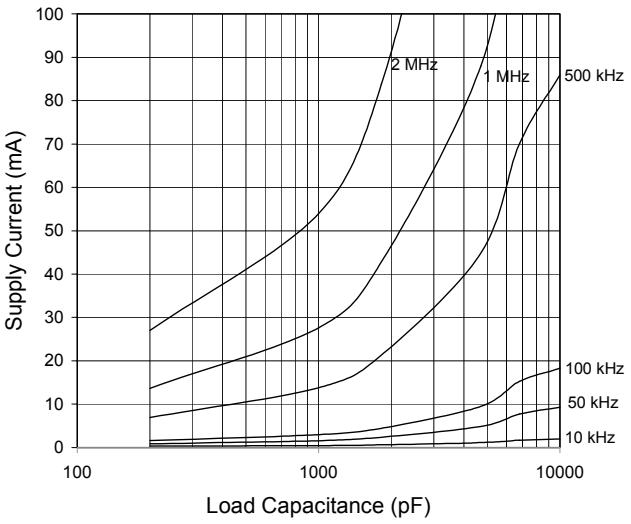


Fig. 16 Supply Current vs. Frequency
Vcc = 18V

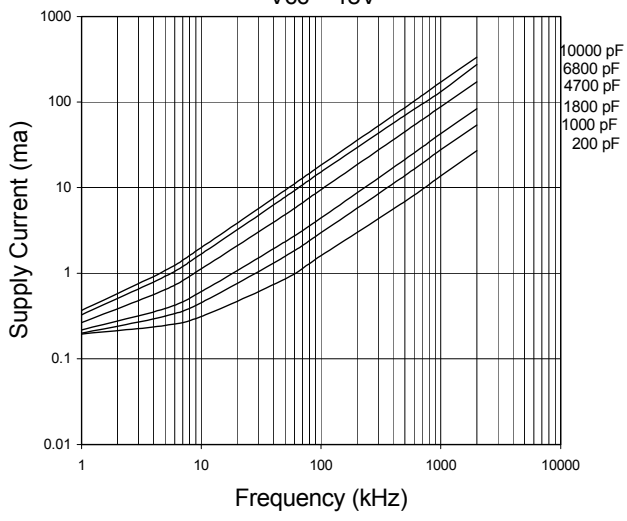


Fig. 17 Supply Current vs. Load Capacitance
Vcc = 35V

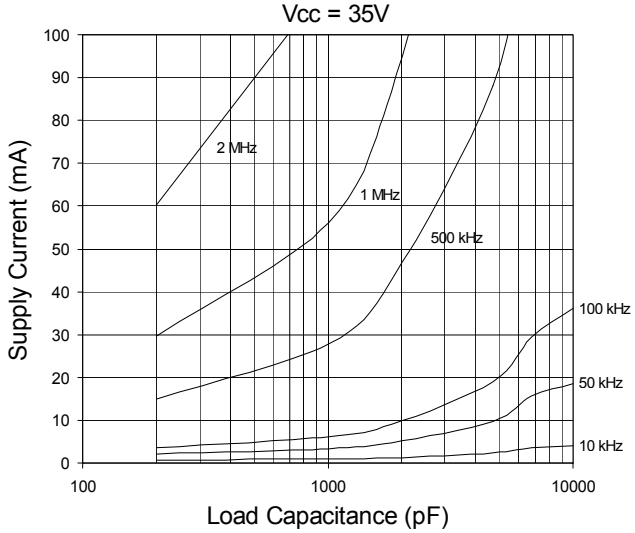


Fig. 18 Supply Current vs. Frequency
Vcc = 35V

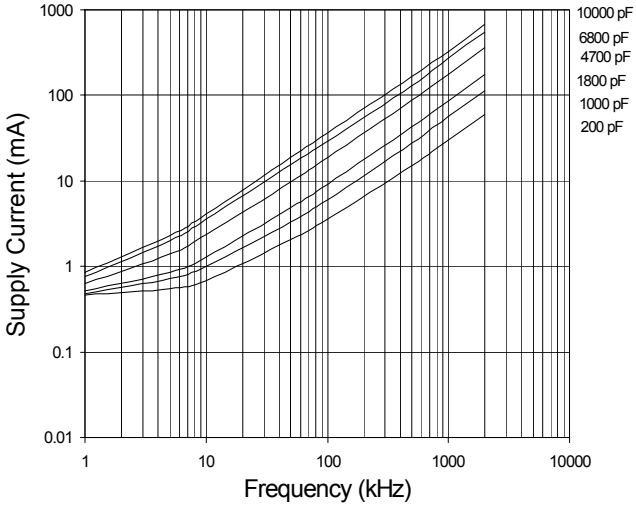


Fig. 19 Propagation Delay vs. Supply Voltage
C_L = 1800pF V_{in} = 5V@1kHz

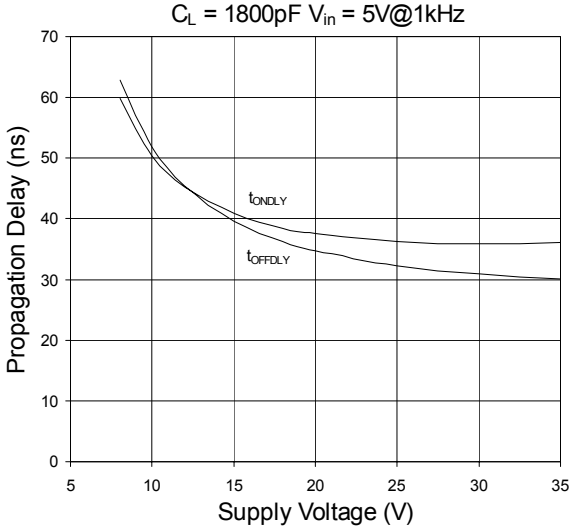


Fig. 20 Propagation Delay vs. Input Voltage
C_L = 1800pF V_{cc} = 15V

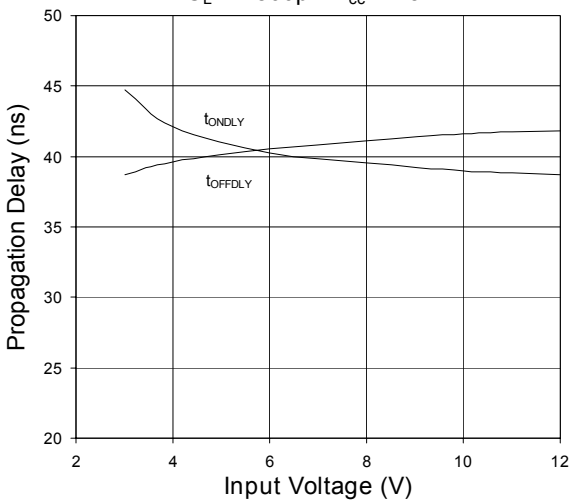


Fig. 21 Propagation Delay Times vs. Temperature
C_L = 1000pF, V_{cc} = 18V

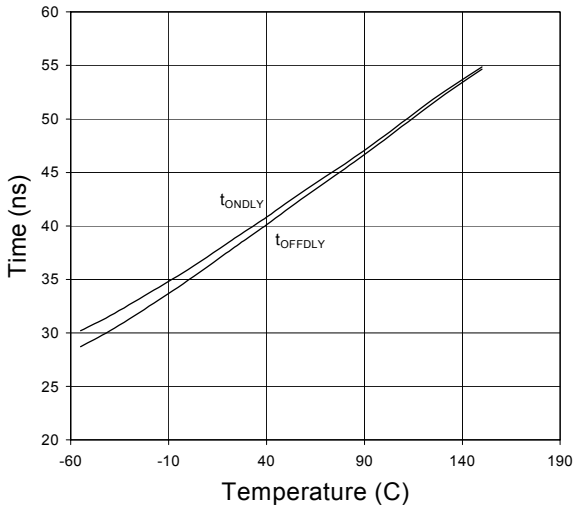


Fig. 22 Quiescent Supply Current vs. Temperature
V_{cc} = 18V, V_{in} = 5V@1kHz, C_L = 1000pF

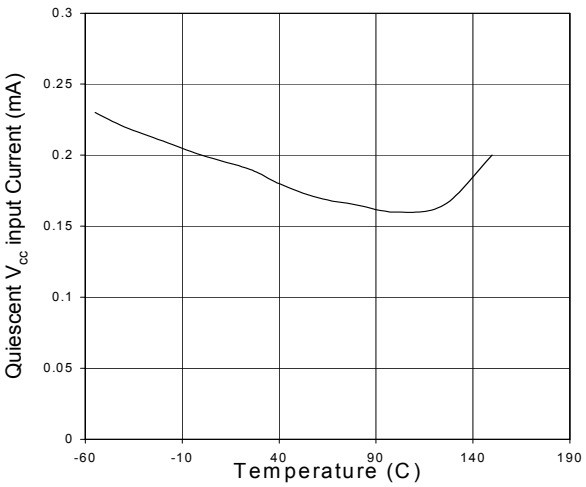


Fig. 23 High State Ouput Resistance vs. Supply Voltage

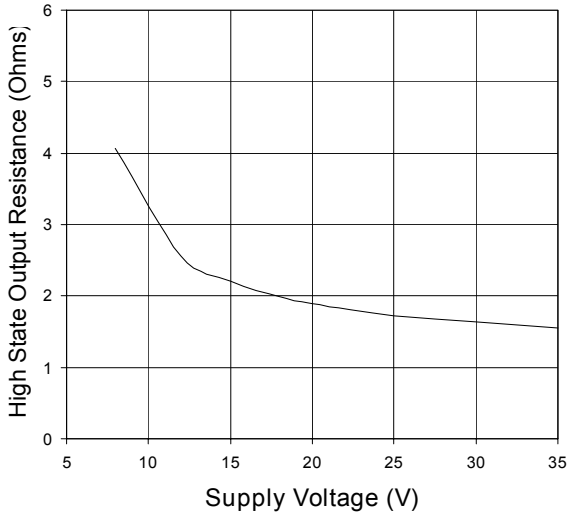


Fig. 24 Low State Output Resistance vs. Supply Voltage

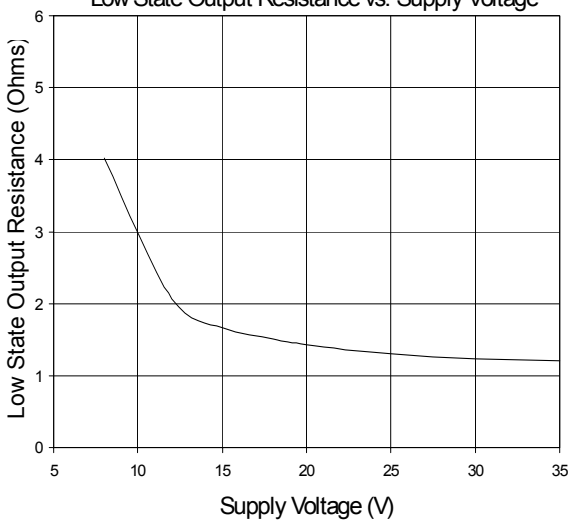


Fig. 25 V_{cc} vs. P Channel Output Current

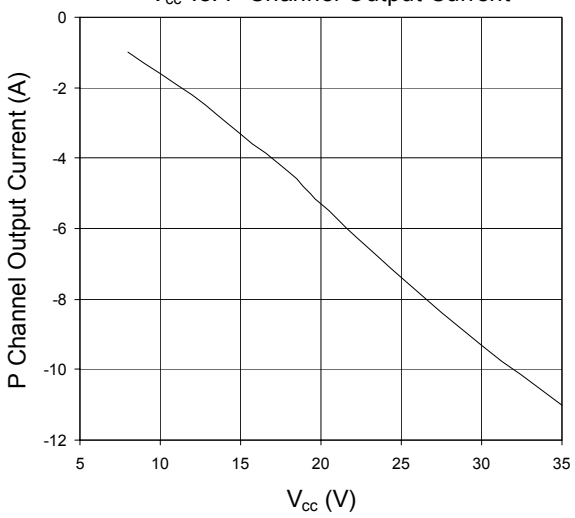


Fig. 26 Vcc vs. N Channel Ouput Current

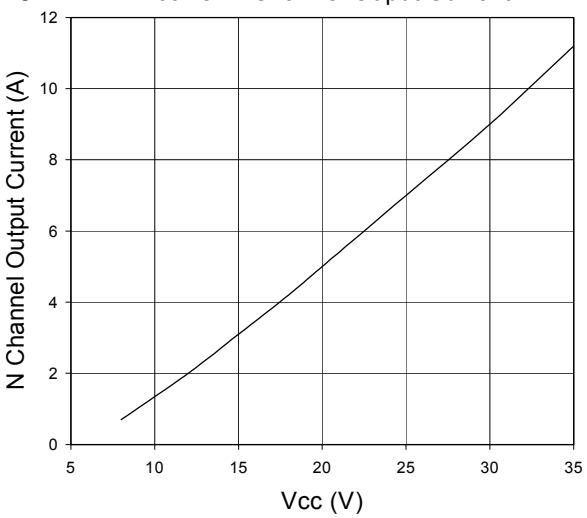


Fig. 27 P Channel Output Current vs. Temperature
V_{cc} = 18V, C_L = 1000pF

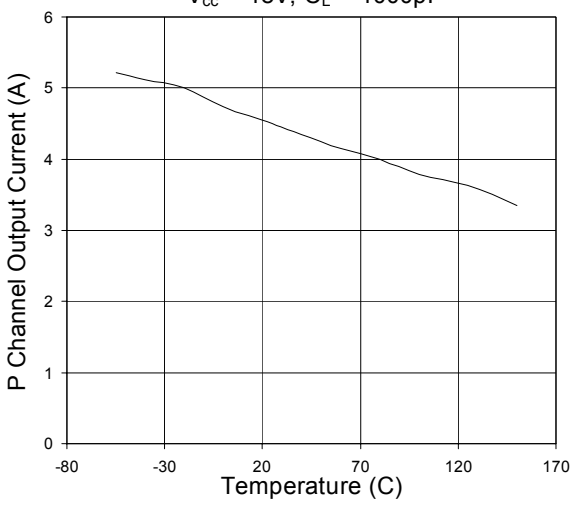
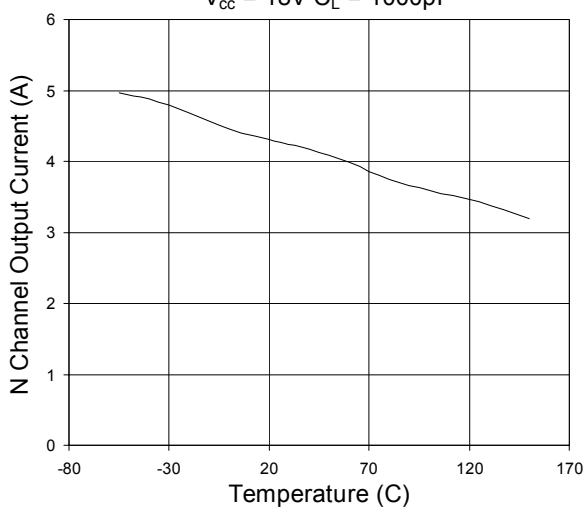
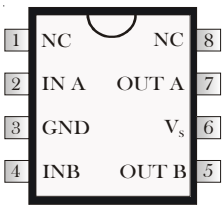


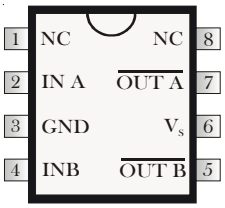
Fig. 28 N Channel Output Current vs. Temperature
V_{cc} = 18V C_L = 1000pF



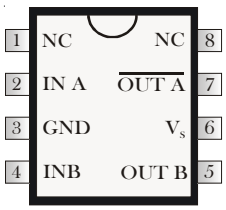
PIN CONFIGURATIONS



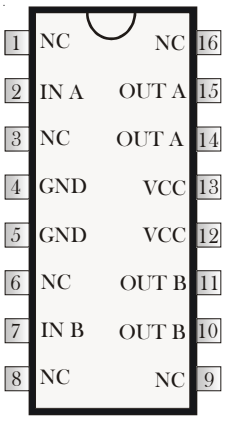
8 Lead PDIP (PI)
8 Pin SOIC (SI)
IXDN404



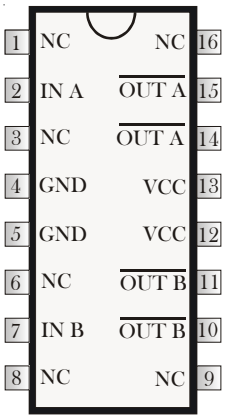
8 Lead PDIP (PI)
8 Pin SOIC (SI)
IXDI404



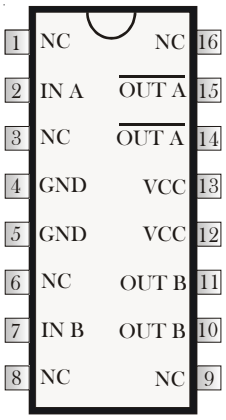
8 Lead PDIP (PI)
8 Pin SOIC (SI)
IXDF404



16 Pin SOIC
IXDN404SI-16



16 Pin SOIC
IXDI404SI-16



16 Pin SOIC
IXDF404SI-16

Supply Bypassing, Grounding Practices And Output Lead inductance

When designing a circuit to drive a high speed MOSFET utilizing the IXDN404/IXDI404/IXDF404, it is very important to observe certain design criteria in order to optimize performance of the driver. Particular attention needs to be paid to **Supply Bypassing**, **Grounding**, and minimizing the **Output Lead Inductance**.

Say, for example, the IXDN404 is being used to charge a 2500pF capacitive load from 0 to 25 volts in 25ns.

Using the formula: $I = \Delta V\ C / \Delta t$, where ΔV=25V C=2500pF & Δt=25ns, one can determine that to charge 2500pF to 25 volts in 25ns will take a constant current of 2.5A. (In reality, the charging current won't be constant and will peak somewhere around 4A).

SUPPLY BYPASSING

In order for the design to turn the load on properly, the IXDN404 must be able to draw this 2.5A of current from the power supply in the 25ns. This means that there must be very low impedance between the driver and the power supply. The most common method of achieving this low impedance is to bypass the power supply at the driver with a capacitance value that is a magnitude larger than the load capacitance. Usually, this would be achieved by placing two different types of bypassing capacitors, with complementary impedance curves, very close to the driver itself. (These capacitors should be carefully selected, low inductance, low resistance, high-pulse current-service capacitors). Lead lengths may radiate at high frequency due to inductance, so care should be taken to keep the lengths of the leads between these bypass capacitors and the IXDN404 to an absolute minimum.

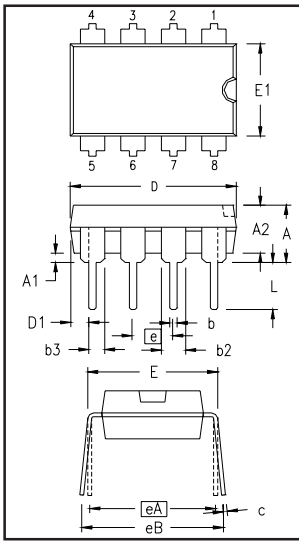
GROUNDING

In order for the design to turn the load off properly, the IXDN404 must be able to drain this 2.5A of current into an adequate grounding system. There are three paths for returning current that need to be considered: Path #1 is between the IXDN404 and its load. Path #2 is between the IXDN404 and its power supply. Path #3 is between the IXDN404 and whatever logic is driving it. All three of these paths should be as low in resistance and inductance as possible, and thus as short as practical. In addition, every effort should be made to keep these three ground paths distinctly separate. Otherwise, the returning ground current from the load may develop a voltage that would have a detrimental effect on the logic line driving the IXDN404.

OUTPUT LEAD INDUCTANCE

Of equal importance to Supply Bypassing and Grounding are issues related to the Output Lead Inductance. Every effort should be made to keep the leads between the driver and its load as short and wide as possible. If the driver must be placed farther than 2" (5mm) from the load, then the output leads should be treated as transmission lines. In this case, a twisted-pair should be considered, and the return line of each twisted pair should be placed as close as possible to the ground pin of the driver, and connected directly to the ground terminal of the load.

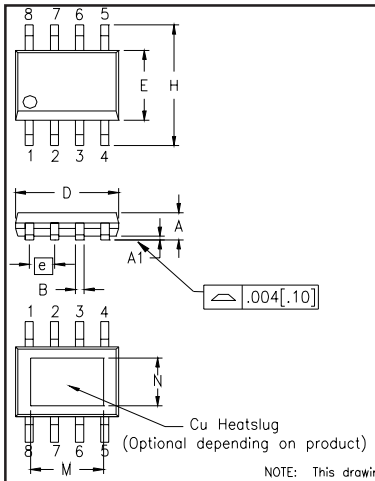
Dimenional Outline: IXDD404PI



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.140	.180	3.56	4.57
A1	.015	.040	0.38	1.02
A2	.125	.145	3.18	3.68
b	.015	.020	0.38	0.51
b2	.055	.065	1.40	1.65
b3	.035	.045	0.89	1.14
c	.009	.012	0.23	0.30
D	.355	.400	9.02	10.16
D1	.010	.040	0.25	1.02
E	.300	.325	7.62	8.26
E1	.240	.270	6.10	6.86
e	.100 BSC		2.54 BSC	
eA	.300 BSC		7.62 BSC	
eB	.300	.430	7.62	10.92
L	.120	.140	3.05	3.56

NOTE: THIS DRAWING MEETS ALL REQUIREMENT OF JEDEC OUTLINES MS-001 BA.

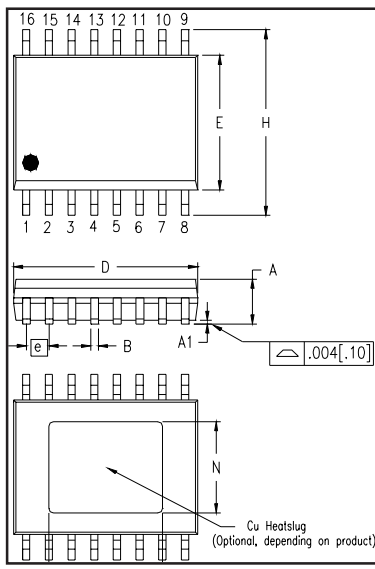
Dimenional Outlines: IXDD404SI-CT and IXDD404SIA



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.053	.069	1.35	1.75
A1	.004	.010	0.10	0.25
B	.013	.020	0.33	0.51
C	.008	.010	0.19	0.25
D	.189	.197	4.80	5.00
E	.150	.157	3.80	4.00
e	.050BSC		1.27BSC	
H	.228	.244	5.80	6.20
h	.010	.020	0.25	0.50
L	.016	.050	0.40	1.27
M	.135	.155	3.43	3.94
N	.095	.115	2.41	2.92
α	0°	8°	0°	8°

NOTE: This drawing will meet all dimensions requirement of JEDEC MS-012 AA.

Dimenional Outlines: IXDD404SI-16CT and IXDD404SIA-16



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.093	.104	2.35	2.65
A1	.004	.012	0.10	0.30
B	.013	.020	0.33	0.51
C	.009	.013	0.23	0.32
D	.398	.413	10.10	10.50
E	.291	.299	7.40	7.60
e	.050BSC		1.27BSC	
H	.394	.419	10.00	10.65
h	.010	.029	0.25	0.75
L	.016	.050	0.40	1.27
M	.240	.260	6.10	6.60
N	.190	.210	4.83	5.33
α	0°	8°	0°	8°

NOTE: 1. This drawing will meet all dimensions requirement of JEDEC MS-013 AA case outline.
2. Cu heatslug is attached to the die attach pad.

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